TRJ 2122

Attorney's Docket No.: 10559-617001/P12856
Intel Corporation

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Gilbert Wolrich et al. Art Unit: 2122
Serial No.: 10/057,723 Examiner:
Filed : January 25, 2002
Assignee : Intel Corporation
Title : CONTEXT PIPELINES

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Dear Sir:

Applicants call attention to the attached Information Disclosure Statement and documents listed on form PTO-1449.

This filing is being made before the receipt of a first Office action on the merits. No fee is required.

The documents are in the English language; hence no concise explanation is necessary per Rule 98(a)(3).

Consideration of the foregoing and enclosures plus the return of a copy of the enclosed form PTO-1449 with the

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I hereby certify under 37 CFR §1.8(a) that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage on the date indicated below and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

November 30, 2004
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Examiner's initials in the left column per MPEP 609 are earnestly solicited along with an early action on the merits.

Please apply any additional charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: November 30, 2004

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Substitute Form PTO-1449 (Modified)	U.S. Department of Commerce Patent and Trademark Office	Attorney's Docket No. 10559-617001	Application No. 10/057,723
Information Disclosure Statement by Applicant (Use several sheets if necessary) (37 CFR 1.98(b))		Applicant Gilbert Wolrich et al.	
		Filing Date January 25, 2002	Group Art Unit 2122

U.S. Patent Documents

Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
	AA	09/473,571	12/28/1999	Wolrich et al.			
	AB	09/475,614	12/30/1999	Wolrich at al.			
	AC						

Foreign Patent Documents or Published Foreign Patent Applications

Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation Yes	Translation No
	AD	WO 94/15287	07/1994	WIPO				
	AE	WO 97/38372	10/1997	WIPO				
	AF	WO 01/16782	03/2001	WIPO				
	AG	WO 01/16770	03/2001	WIPO				
	AH	WO 01/16769	03/2001	WIPO				
	AI	WO 01/15718	03/2001	WIPO				
	AJ	WO 01/48619	07/2001	WIPO				
	AK	WO 01/48606	07/2001	WIPO				
	AL	WO 01/48596	07/2001	WIPO				
	AM	WO 01/50679	07/2001	WIPO				
	AN	WO 01/50247	07/2001	WIPO				
	AO	WO 01/95101	12/2001	WIPO				
	AP	0 379 709	08/1990	Europe				
	AQ	0 464 715	01/1992	Europe				
	AR	0 633 678	01/1995	Europe				
	AS	0 745 933	12/1996	Europe				
	AT	0 809 180	11/1997	Europe				
	AU	1 148 414	10/2001	Europe				
	AV	59-111533	06/1984	Japan				
	AW							

Examiner Signature	Date Considered

EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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Other Documents (include Author, Title, Date, and Place of Publication)		
Examiner Initial	Desig. ID	Document
	AX	Byrd et al., "Multithread Processor Architectures," *IEEE Spectrum*, Vol. 32, No. 8, New York, 1 August 1995, pp. 38-46.
	AY	Doyle et al., *Microsoft Press Computer Dictionary*, 2nd ed., Microsoft Press, Redmond, Washington, USA, 1994, p. 326.
	AZ	Fillo et al., "The M-Machine Multicomputer," IEEE Proceedings of MICRO-28, 1995, pp. 146-156.
	AAA	Gomez et al., "Efficient Multithreaded User-Space Transport for Network Computing: Design and Test of the TRAP Protocol," *Journal of Parallel and Distributed Computing*, Academic Press, Duluth, Minnesota, USA, vol. 40, no. 1, 10 January 1997, pp. 103-117.
	ABB	Haug et al., "Reconfigurable hardware as shared resource for parallel threads," IEEE Symposium on FPGAs for Custom Computing Machines, 1998.
	ACC	Hauser et al., "Garp: a MIPS processor with a reconfigurable coprocessor," Proceedings of the 5th Annual 1EEE Symposium on Field-Programmable Custom Computing Machines, 1997.
	ADD	Hyde, R., "Overview of Memory Management," *Byte*, vol. 13, no. 4, 1998, pp. 219-225.
	AEE	Litch et al., "StrongARMing Portable Communications," IEEE Micro, 1998, pp. 48-55.
	AFF	Moors, et al., "Cascading Content-Addressable Memories", *IEEE Micro*, 12(3):56-66 (1992).
	AGG	Schmidt et al., "The Performance of Alternative Threading Architectures for Parallel Communication Subsystems," Internet Document, *Online!*, 13 November 1998.
	AHH	Shah, Niraj, "Understanding Network Processors", *Masters Thesis Submitted to the University of California, Berkeley*, September 4, 2001.
	AII	Thistle et al., "A Processor Architecture for Horizon," IEEE, 1998, pp. 35-41.
	AJJ	Tremblay et al., "A Three Dimensional Register File for Superscalar Processors," IEEE Proceedings of the 28th Annual Hawaii International Conference on System Sciences, 1995, pp. 191-201.
	AKK	Trimberger et al, "A time-multiplexed FPGA," Proceedings of the 5th Annual IEEE Symposium on Field-Programmable Custom Computing Machines," 1998.
	ALL	Turner et al., "Design of a High Performance Active Router," Internet Document, *Online*, 18 March 1999.
	AMM	Vibhatavanijt et al., "Simultaneous Multithreading-Based Routers," Proceedings of the 2000 International Conference of Parallel Processing, Toronto, Ontario, Canada, 21-24 August 2000, pp. 362-359.
	ANN	Wazlowski et al., "PRSIM-II computer and architecture," IEEE Proceedings, Workshop on FPGAs for Custom Computing Machines, 1993.
	AOO	International Search Report from PCT/US03/01578; mailed February 19, 2004 (4 pages).
	APP	International Search Report from PCT/US03/01580; mailed April 21, 2004. (4 pages)

Examiner Signature	Date Considered
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